19-3577; Rev 1; 8/05

10/100/1000 Base-T Ethernet LAN Switch

General Description

The MAX4890/MAX4891/MAX4892 high-speed analog switches meet the needs of 10/100/1000 Base-T applications. These devices switch the signals from two interface transformers and connect the signals to a single 10/100/1000 Base-T Ethernet PHY, simplifying docking station design and reducing manufacturing costs. The MAX4890/MAX4891/MAX4892 can also route signals from a common interface transformer to two different boards in board-redundancy applications.

The MAX4890/MAX4891/MAX4892 switches provide an extremely low capacitance and on-resistance to meet Ethernet insertion and return-loss specifications. The MAX4891/MAX4892 feature one and three built-in LED switches, respectively.

The MAX4890/MAX4891/MAX4892 are available in space-saving 32- and 36-lead TQFN packages, significantly reducing the required PC board area. These devices operate over the -40°C to +85°C temperature range.

Applications

Notebooks and Docking Stations

Servers and Routers with Ethernet Interfaces

Board-Level Redundancy Protection

SONET/SDH Signal Routing

T3/E3 Redundancy Protection

Video Switching

Typical Operating Circuit appears at end of data sheet.

Features

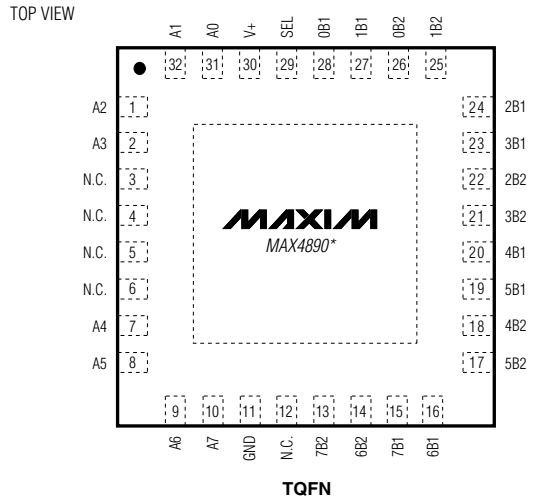
- **Single +3.0V to +3.6V Power-Supply Voltage**
- **Low On-Resistance (R_{ON}): 4Ω (typ), 6.5Ω (max)**
- **Ultra-Low On-Capacitance (C_{ON}): 6.5pF (typ)**
- **Low < 200ps Bit-to-Bit Skew**
- **-3dB Bandwidth: 1GHz**
- **Optimized Pin-Out for Easy Transformer and PHY Interface**
- **Built-In LED Switches for Switching Indicators to Docking Station**
- **Low 450µA (max) Quiescent Current**
- **Bidirectional 8 to 16 Multiplexer/Demultiplexer**
- **Space-Saving Packages**
  32-Pin, 5mm x 5mm, TQFN Package
  36-Pin, 6mm x 6mm, TQFN Package

Ordering Information

PART	PIN-PACKAGE	LED SWITCHES	PKG CODE
MAX4890ETJ	32 TQFN	—	T-3255-4
MAX4891ETJ	32 TQFN	1	T-3255-4
MAX4892ETX	36 TQFN	3	T-3666-3

All devices are available in the -40°C to +85°C operation temperature range.

Pin Configurations



TQFN

Pin Configurations continued at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

V+ ..... -0.3V to +4V
SEL (Note 1) ..... -0.3V to (V+ +0.3V)
A_, _B_, LED_, _LED_ ..... -0.3V to (V+ +0.3V)
Continuous Current (A_ to _B_) .....±120mA
Continuous Current (LED_ to _LED_) ..... ±30mA
Peak Current (A_ to _B_)
(pulsed at 1ms, 10% duty cycle) ..... ±240mA

Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 34.5mW/°C above +70°C) 2.76W
36-Pin TQFN (derate 26.3mW/°C above +70°C) 2.11W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Signals on SEL, exceeding V+ or GND, are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +3V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SWITCH							
On-Resistance	R_{ON}	V+ = 3V, $I_{A\_}$ = -40mA, 1.5V ≤ $V_{A\_}$ ≤ V+	T_A = +25°C		4	5.5	Ω
			T_{MIN} to T_{MAX}			6.5	
On-Resistance LED Switches	R_{ONLED}	V+ = 3V, $I_{\_LED\_}$ = -40mA, 1.5V ≤ $V_{A\_}$ ≤ V+, MAX4891/MAX4892				40	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V+ = 3V, $I_{A\_}$ = -40mA, 1.5V ≤ $V_{A\_}$ ≤ V+ (Note 3)	T_A = +25°C		0.5	1.5	Ω
			T_{MIN} to T_{MAX}			2	
On-Resistance Flatness	$R_{FLAT(ON)}$	V+ = 3V, $I_{A\_}$ = -40mA, $V_{A\_}$ = 1.5V, 2.7V			0.01		Ω
Off-Leakage Current	$I_{LA\_(OFF)}$	V+ = 3.6V, $V_{A\_}$ = 0.3V, 3.3V $V_{\_B1}$ or $V_{\_B2}$ = 3.3V, 0.3V		-1		+1	µA
On-Leakage Current	$I_{LA\_(ON)}$	V+ = 3.6V, $V_{A\_}$ = 0.3V, 3.3V $V_{\_B1}$ or $V_{\_B2}$ = 0.3V, 3.3V or floating		-1		+1	
ESD PROTECTION							
ESD Protection		Human Body Model			±2		kV
SWITCH AC PERFORMANCE							
Insertion Loss	I_{LOS}	Insertion loss with typical transformer, R_L = 100Ω, 1MHz < f < 100MHz, Figure 1 (Note 3)			0.6		dB
Return Loss	R_{LOS1}	Return loss with typical transformer, R_L = 100Ω, return loss, f in MHz, Figure 2 (Note 3)	1MHz < f < 40MHz		-19		dB
	R_{LOS2}		40MHz < f < 100MHz		-13 +20log (f/80)		

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +3V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3V, T_A = +25°C.) (Note 2)

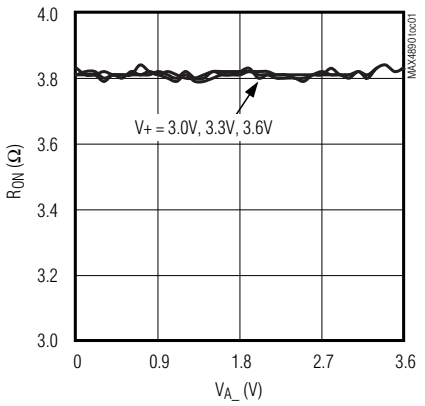
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Crosstalk	V_{CT1}	Any switch to any switch R_L = 100Ω, Figure 3	1MHz < f < 30MHz		-45		dB
	V_{CT2}		30MHz < f < 60MHz		-40		
	V_{CT3}		60MHz < f < 100MHz		-35		
Differential Crosstalk	V_{DCT1}	R_L = 100Ω, Figure 4	1MHz < f < 30MHz		-60		dB
	V_{DCT2}		30MHz < f < 60MHz		-55		
	V_{DCT3}		60MHz < f < 100MHz		-50		
SWITCH DYNAMICS							
On-Channel -3dB Bandwidth	BW	R_L = 100Ω, Differential pair			1000		MHz
Off-Capacitance	C_{OFF}	f = 1MHz, _B_ inputs			3.5		pF
On-Capacitance	C_{ON}	f = 1MHz, _B_ inputs			6.5		pF
Off-Capacitance, LED Switches	C_{OFFLED}	f = 1MHz, _LED inputs			20		pF
On-Capacitance, LED Switches	C_{ONLED}	f = 1MHz, _LED inputs			22		pF
Turn-On Time	t_{ON}	$V_{A\_}$ = 1V, Figure 5			25	50	ns
Turn-Off Time	t_{OFF}	$V_{A\_}$ = 1V, Figure 5			20	40	ns
Propagation Delay	t_{PLH}, t_{PHL}	C_L = 10pF, Figure 6			0.15		ns
Output Skew Between Ports	$t_{SK(o)}$	Skew between A4 and A5 and any other port, Figure 7			0.01		ns
Output Skew Same Port	$t_{SK(p)}$	Skew between opposite transitions in same port			0.07		ns
SWITCH LOGIC							
Input-Voltage Low	V_{IL}					0.8	V
Input-Voltage High	V_{IH}			2.0			
Input-Logic Hysteresis	V_{HYST}				100		mV
Input Leakage Current	I_{SEL}	V+ = 3.6V, V_{SEL} = 0 or V+		-5		+5	uA
Operating Supply-Voltage Range	V+			3		3.6	V
Quiescent Supply Current	I+	V+ = 3.6V, V_{SEL} = 0 or V+			280	450	µA

Note 2: Specifications at -40°C are guaranteed by design.
Note 3: Guaranteed by design.

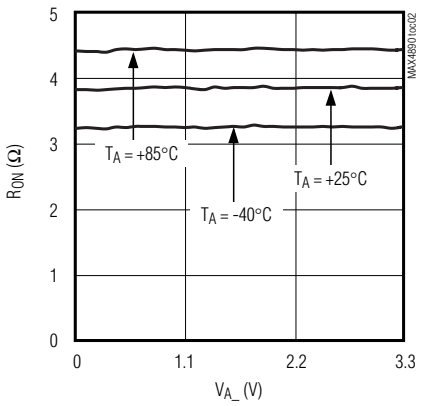
Typical Operating Characteristics

(V+ = 3.3V, T_A = +25°C, unless otherwise noted.)

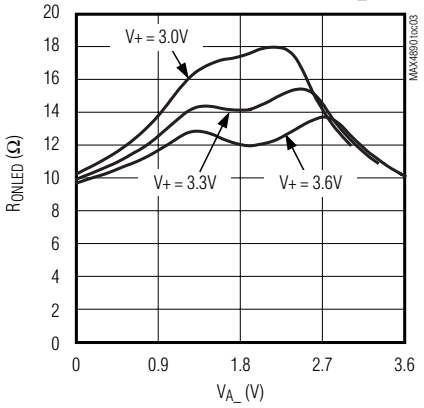
ON-RESISTANCE vs. $V_{A\_}$



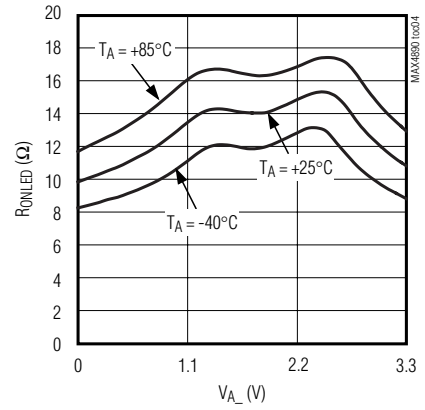
ON-RESISTANCE vs. $V_{A\_}$



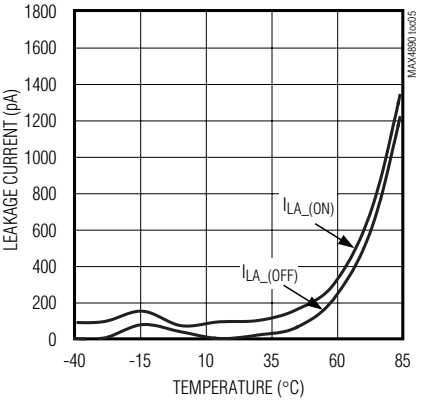
LED_ ON-RESISTANCE vs. $V_{A\_}$



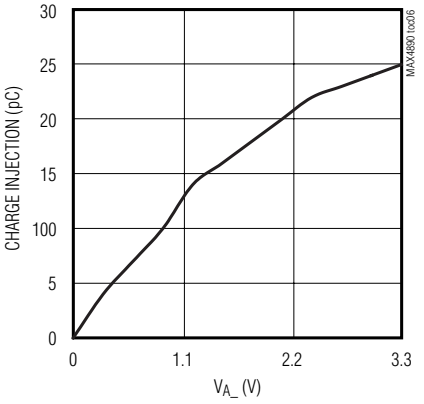
LED_ ON-RESISTANCE vs. TEMPERATURE



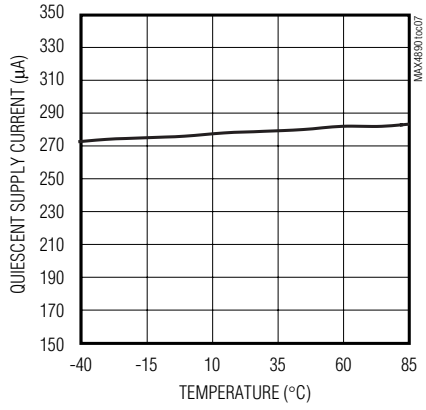
LEAKAGE CURRENT vs. TEMPERATURE



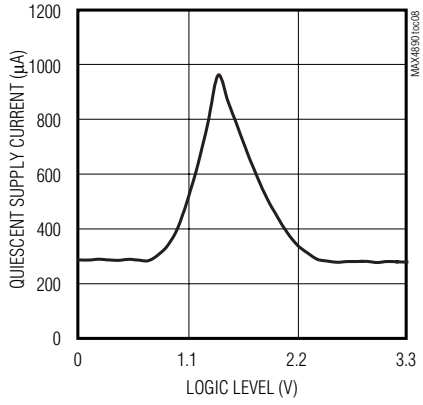
CHARGE INJECTION vs. $V_{A\_}$



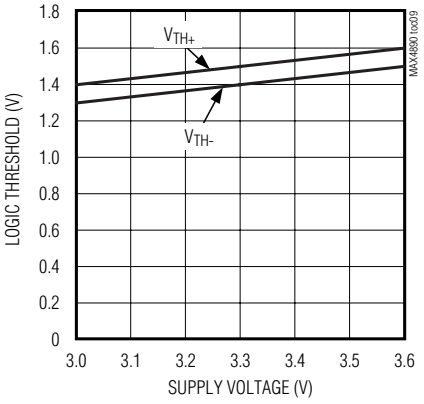
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



QUIESCENT SUPPLY CURRENT vs. LOGIC LEVEL



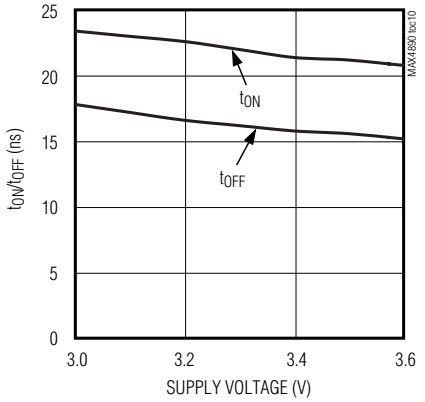
LOGIC THRESHOLD vs. SUPPLY VOLTAGE



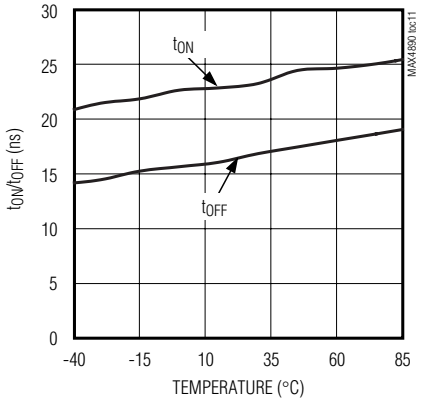
Typical Operating Characteristics (continued)

(V+ = 3.3V, T_A = +25°C, unless otherwise noted.)

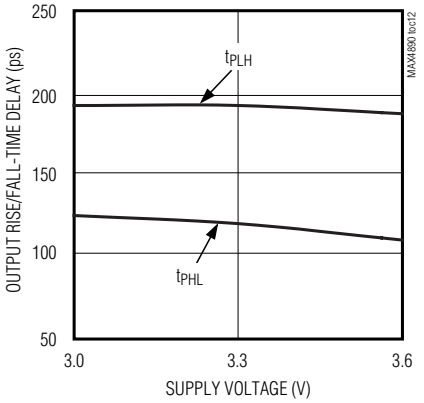
TURN-ON/-OFF TIME vs. SUPPLY VOLTAGE



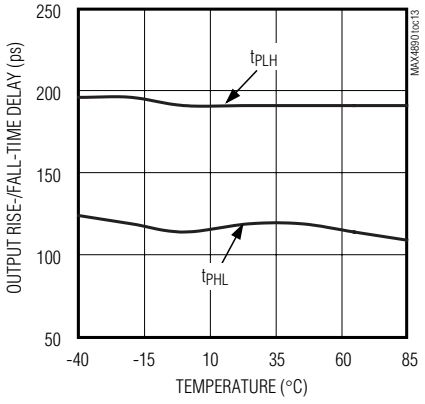
TURN-ON/-OFF TIME vs. TEMPERATURE



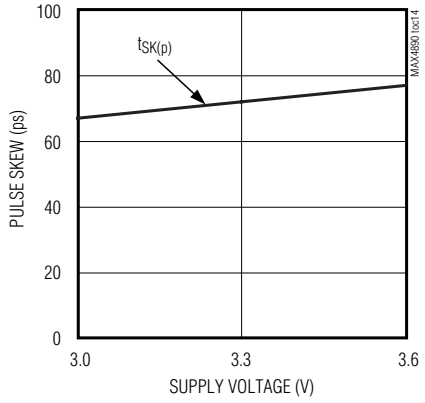
RISE-/FALL-TIME PROPAGATION DELAY vs. SUPPLY VOLTAGE



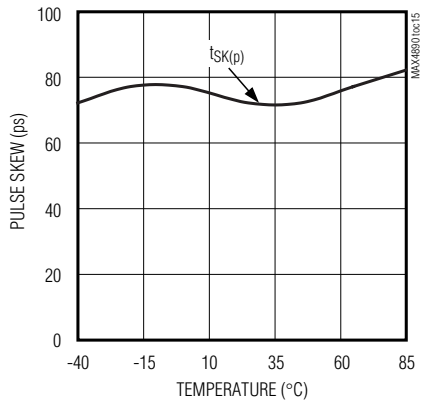
RISE-/FALL-TIME PROPAGATION DELAY vs. TEMPERATURE



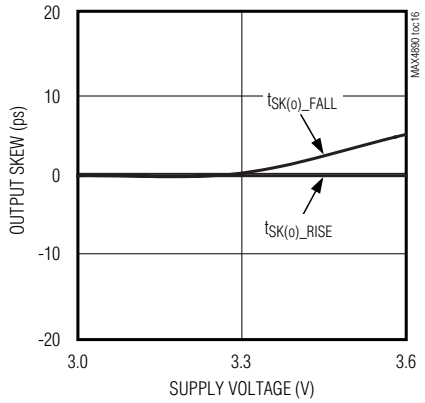
PULSE SKEW vs. SUPPLY VOLTAGE



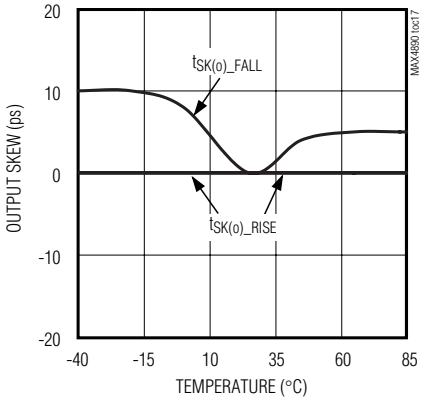
PULSE SKEW vs. TEMPERATURE



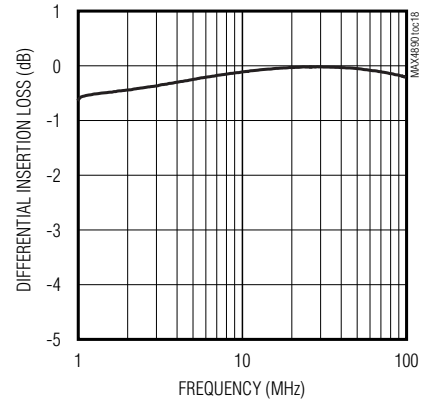
OUTPUT SKEW vs. SUPPLY VOLTAGE



OUTPUT SKEW vs. TEMPERATURE



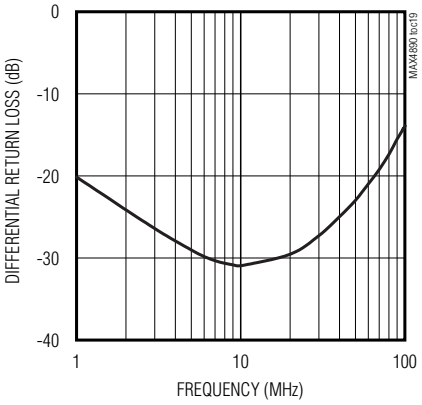
DIFFERENTIAL INSERTION LOSS vs. FREQUENCY



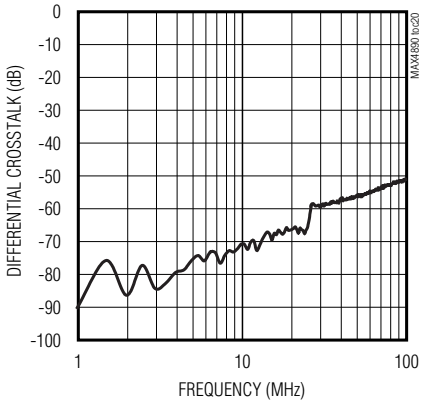
Typical Operating Characteristics (continued)

(V+ = 3.3V, T_A = +25°C, unless otherwise noted.)

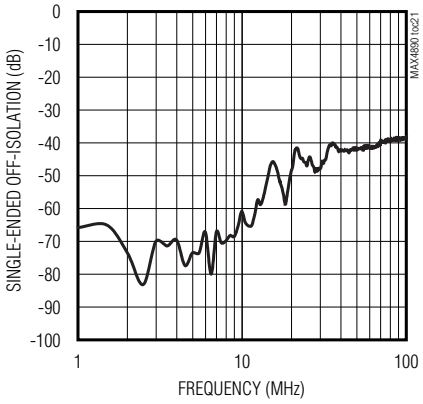
DIFFERENTIAL RETURN LOSS vs. FREQUENCY



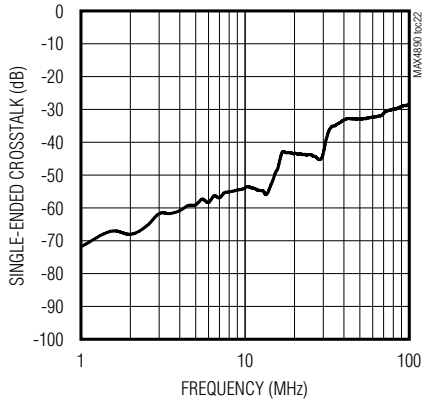
DIFFERENTIAL CROSSTALK vs. FREQUENCY



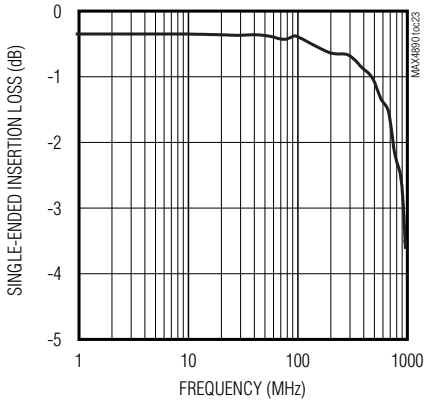
SINGLE-ENDED OFF-ISOLATION vs. FREQUENCY



SINGLE-ENDED CROSSTALK vs. FREQUENCY



SINGLE-ENDED INSERTION LOSS vs. FREQUENCY



Pin Description

PIN			NAME	FUNCTION
MAX4890	MAX4891	MAX4892		
31, 32, 1, 2, 7–10	31, 32, 1, 2, 7–10	36, 1, 2, 3, 7–10	A0–A7	Differential PHY Interface Pair. Connects to the Ethernet PHY.
—	3	4	LED0	LED0 Input
—	4	5	0LED1	0LED1 Output. Connects LED0 to 0LED1 when SEL = 0.
—	5	6	0LED2	0LED2 Output. Connects LED0 to 0LED2 when SEL = 1.
3–6, 12	6, 12	—	N.C.	No Connection. Not internally connected.
11	11	11	GND	Ground
—	—	12	LED1	LED1 Input
—	—	13	1LED1	1LED1 Output. Connects LED1 to 1LED1 when SEL = 0.
—	—	14	1LED2	1LED2 Output. Connects LED1 to 1LED2 when SEL = 1.
13, 14, 17, 18, 21, 22, 25, 26	13, 14, 17, 18, 21, 22, 25, 26	15, 16, 19, 20, 23, 24, 28, 29	7B2–0B2	B2 Differential Transformer Pair
15, 16, 19, 20, 23, 24, 27, 28	15, 16, 19, 20, 23, 24, 27, 28	17, 18, 21, 22, 25, 26, 30, 31	7B1–0B1	B1 Differential Transformer Pair
29	29	27	SEL	Select Input. Selects switch connection. See the Truth Table (Table 1).
—	—	32	2LED2	2LED2 Output. Connects LED2 to 2LED2 when SEL = 1.
—	—	33	2LED1	2LED1 Output. Connects LED2 to 2LED1 when SEL = 0.
—	—	34	LED2	LED2 Input
30	30	35	V+	Positive Supply-Voltage Input
EP	EP	EP	EP	Exposed Paddle. Not internally connected. Leave unconnected or connect to ground.

Test Circuits

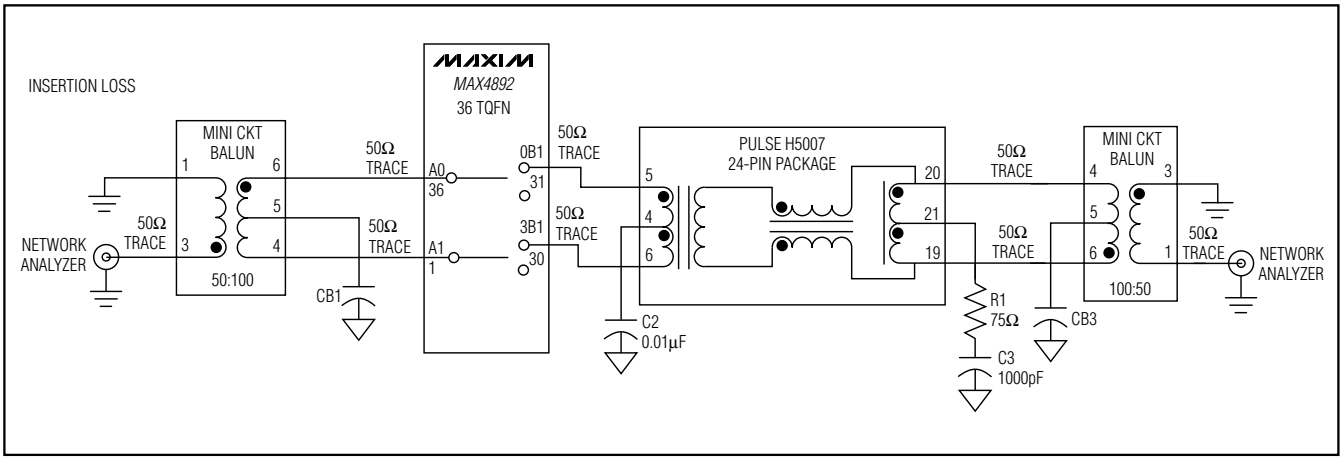


Figure 1. Differential Insertion Loss

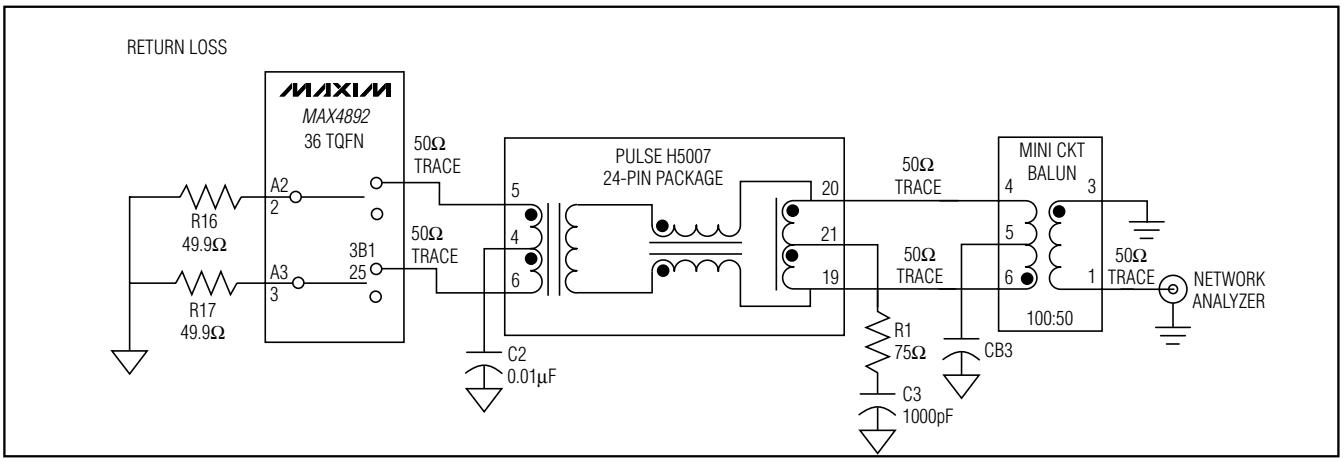


Figure 2. Differential Return Loss

Test Circuits (continued)

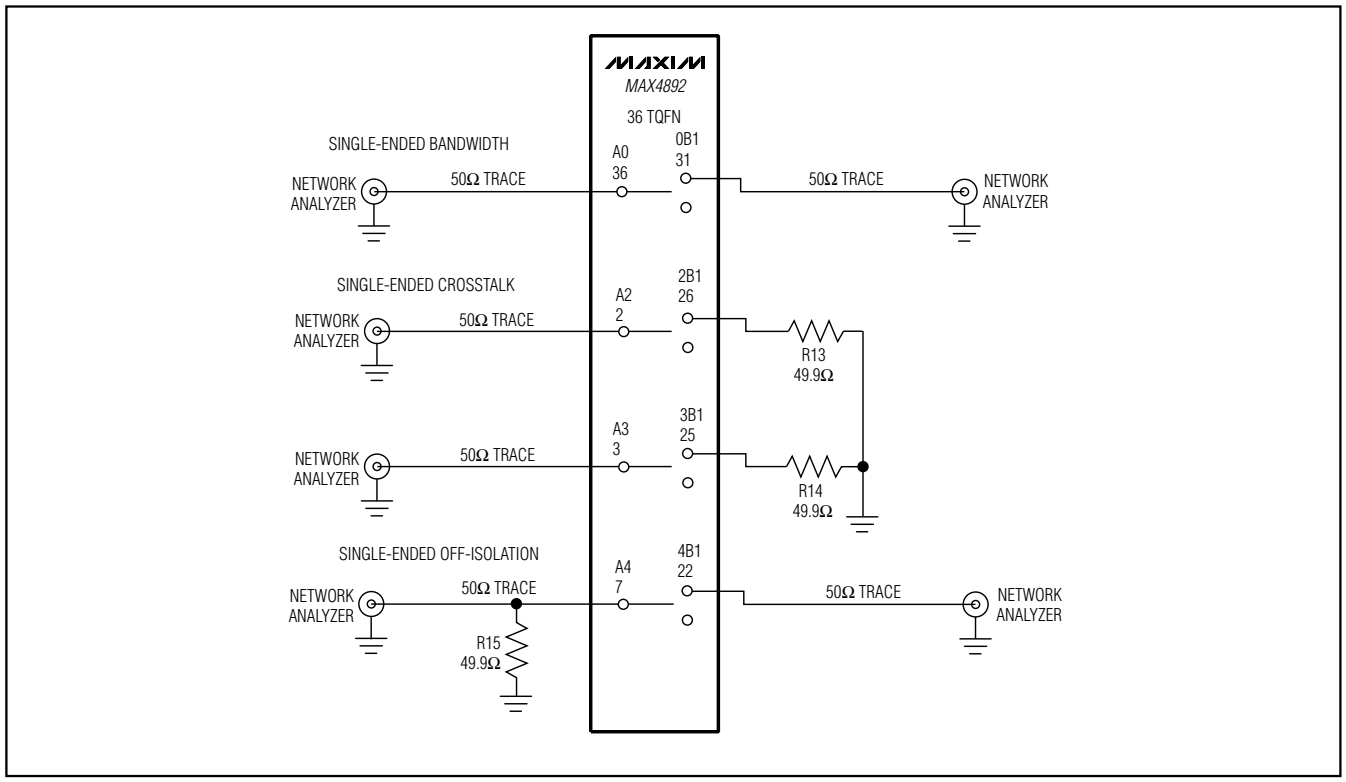


Figure 3. Single-Ended Bandwidth, Crosstalk and Off-Isolation

Detailed Description

The MAX4890/MAX4891/MAX4892 are high-speed analog switches targeted for 10/100/1000 Base-T applications. In a typical application, the MAX4890/MAX4891/MAX4892 switch the signals from two separate interface transformers and connect the signals to a single 10/100/1000 Base-T Ethernet PHY (see the *Typical Operating Circuit*). This configuration simplifies docking station design by avoiding signal reflections associated with unterminated transmission lines in a T configuration. The MAX4891 and MAX4892 also include LED switches that allow the LED output signals to be routed to a docking station along with the Ethernet signals. See the *Functional Diagrams.*

The MAX4890/MAX4891/MAX4892 switches provide an extremely low capacitance and on-resistance to meet Ethernet insertion and return-loss specifications. The MAX4891/MAX4892 feature one and three built-in LED switches, respectively.

The MAX4890/MAX4891/MAX4892 incorporate a unique architecture design utilizing only n-channel switches within the main Ethernet switch, reducing I/O capacitance and channel resistance. An internal two-stage charge pump with a nominal output of 7.5V provides the high voltage needed to drive the gates of the n-channel switches, while maintaining a consistently low R_{ON} throughout the input signal range. An internal bandgap reference set to 1.23V and an internal oscillator running at 2.5MHz provide proper charge-pump operation. Unlike other charge-pump circuits, the MAX4890/MAX4891/MAX4892 include internal flyback capacitors, reducing design time, board space, and cost.

Digital Control Inputs

The MAX4890/MAX4891/MAX4892 provide a single digital control SEL. SEL controls the switches as well as the LED switches as shown in Table 1.

Table 1. Truth Table

SEL	CONNECTION
0	A_ to _B1, LED_ to _LED1
1	A_ to _B2, LED_ to _LED2

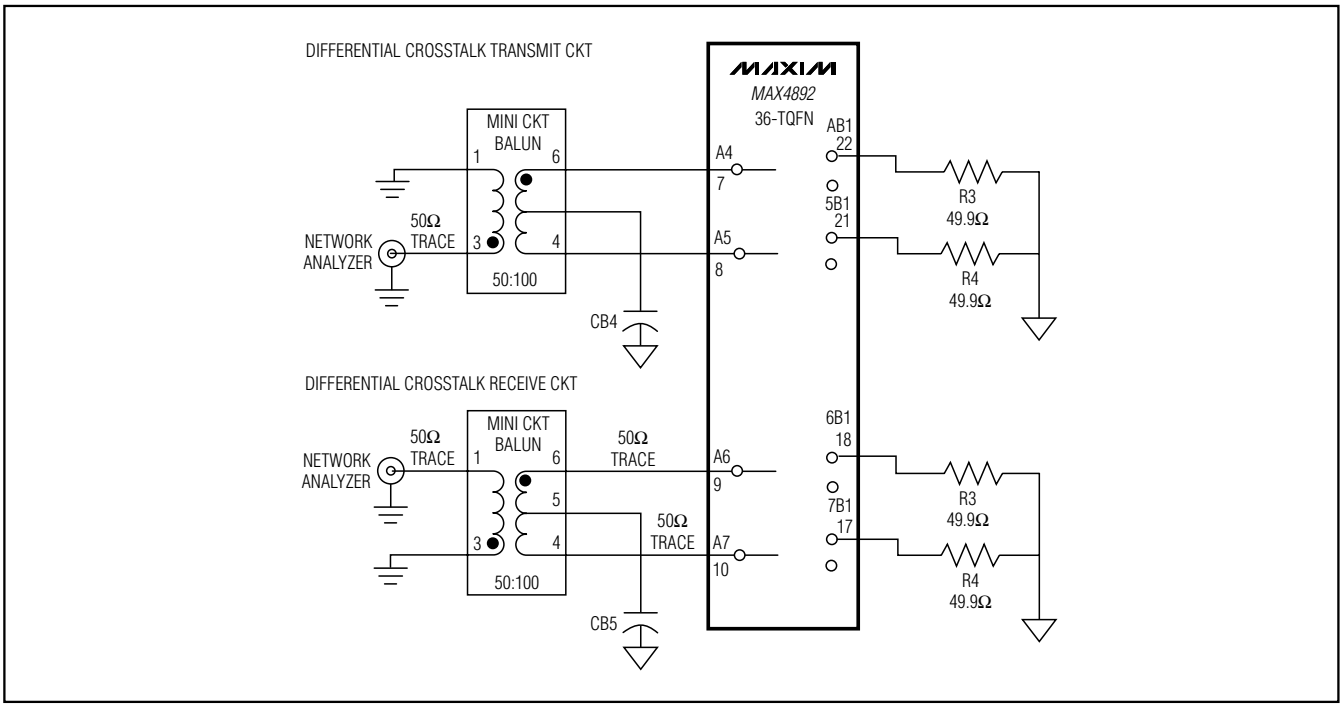


Figure 4. Differential Crosstalk

Analog Signal Levels

The on-resistance of the MAX4890/MAX4891/MAX4892 is very low and stable as the analog input signals are swept from ground to V+ (see the *Typical Operating Characteristics*). The switches are bidirectional, allowing A_ and _B_ to be configured as either inputs or outputs.

ESD Protection

The MAX4890/MAX4891/MAX4892 are characterized using the Human Body Model for ±2kV of ESD protection. Figure 8 shows the Human Body Model, and Figure 9 shows the current waveform the Human Body Model generates when discharged into a low-impedance load. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

Applications Information

Typical Operating Circuit

The *Typical Operating Circuit* depicts the MAX4890/MAX4891/MAX4892 in a 10/100/1000 Base-T docking station application.

Line-Card Redundancy (Ethernet T3/E3)

Figure 10 shows the MAX4890/MAX4891/MAX4892 in a line-card redundancy configuration.

Power-Supply Sequencing and Overvoltage Protection

Caution: Do not exceed the absolute maximum ratings. Stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals, especially if the analog signal is not current limited.

Layout

High-speed switches require proper layout and design procedures for optimum performance. Keep design-controlled-impedance printed circuit board traces as short as possible. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

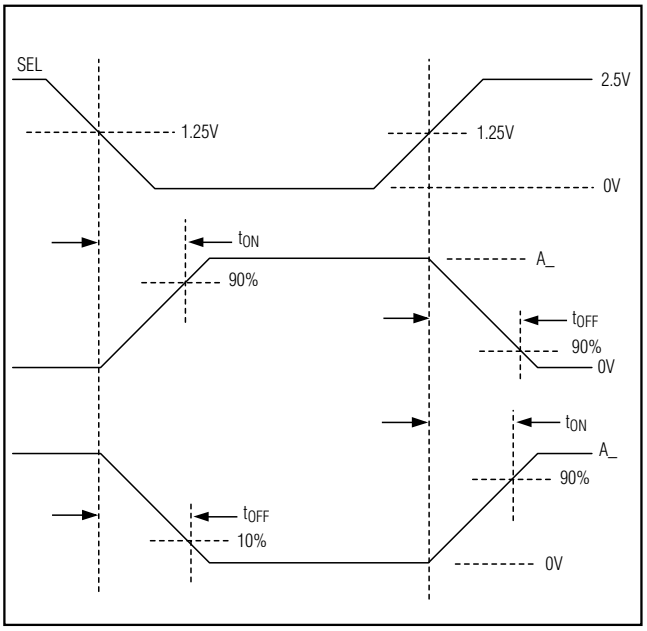


Figure 5. ENABLE and DISABLE Times

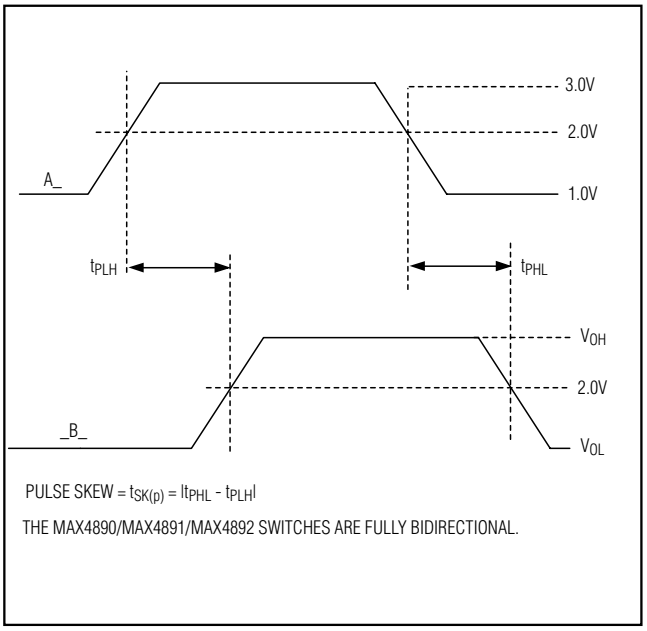


Figure 6. Propagation Delay Times

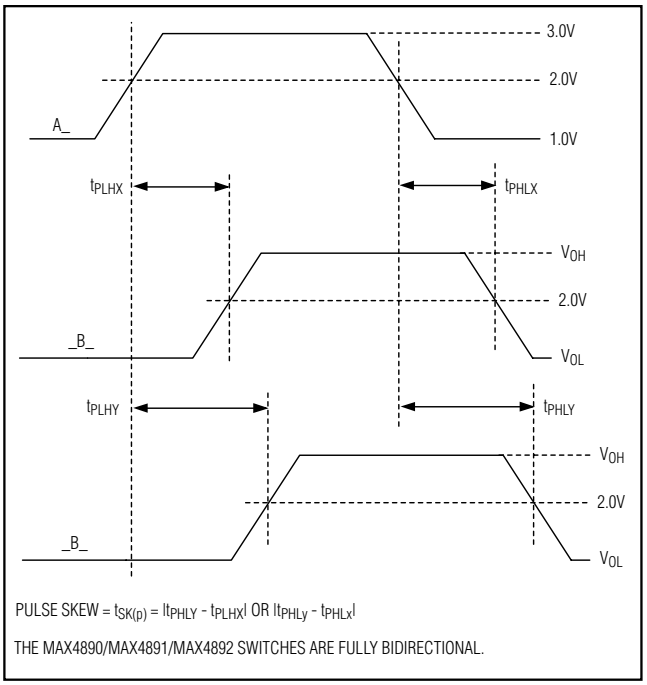


Figure 7. Output Skew

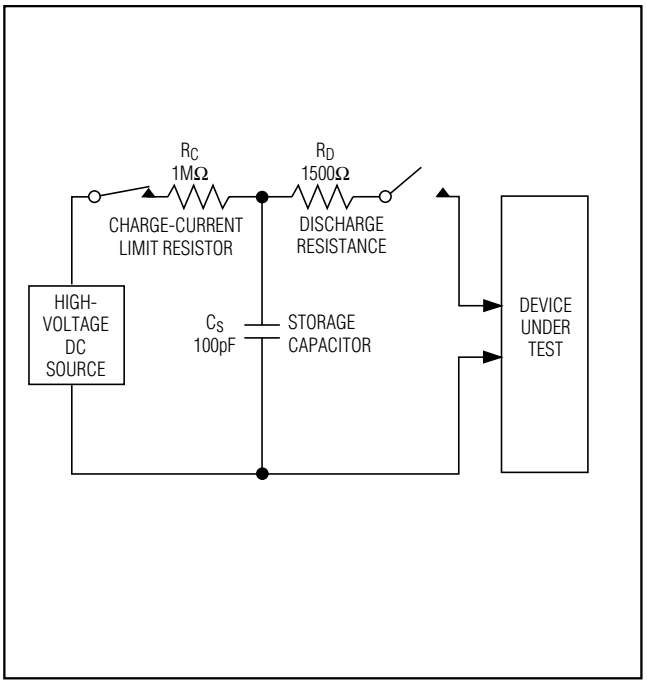


Figure 8. Human Body ESD Test Model

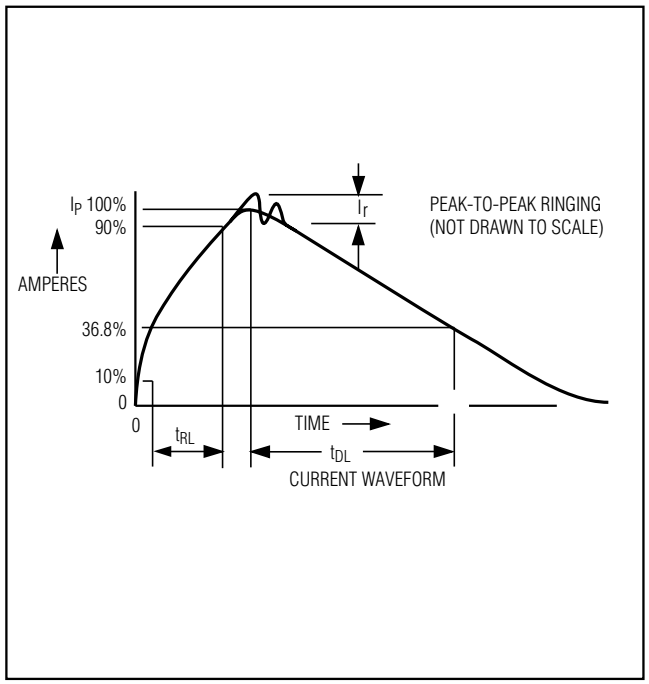


Figure 9. Human Body Model Current Waveform

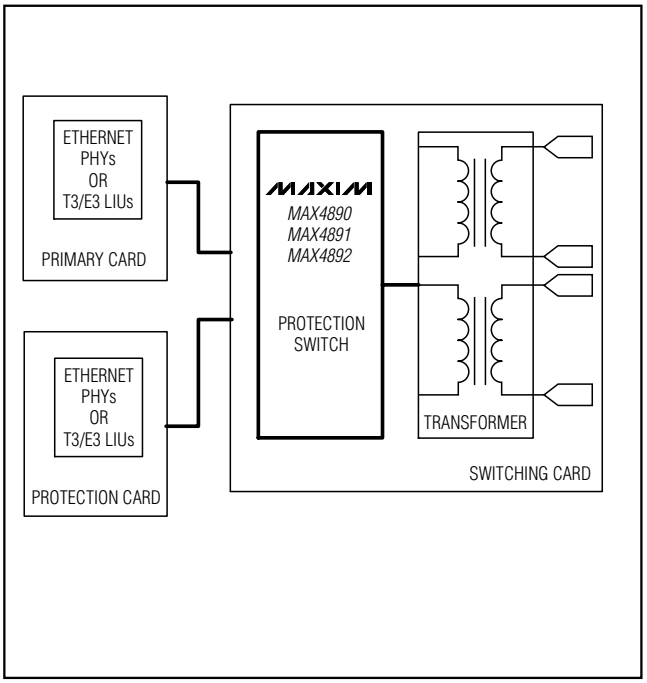
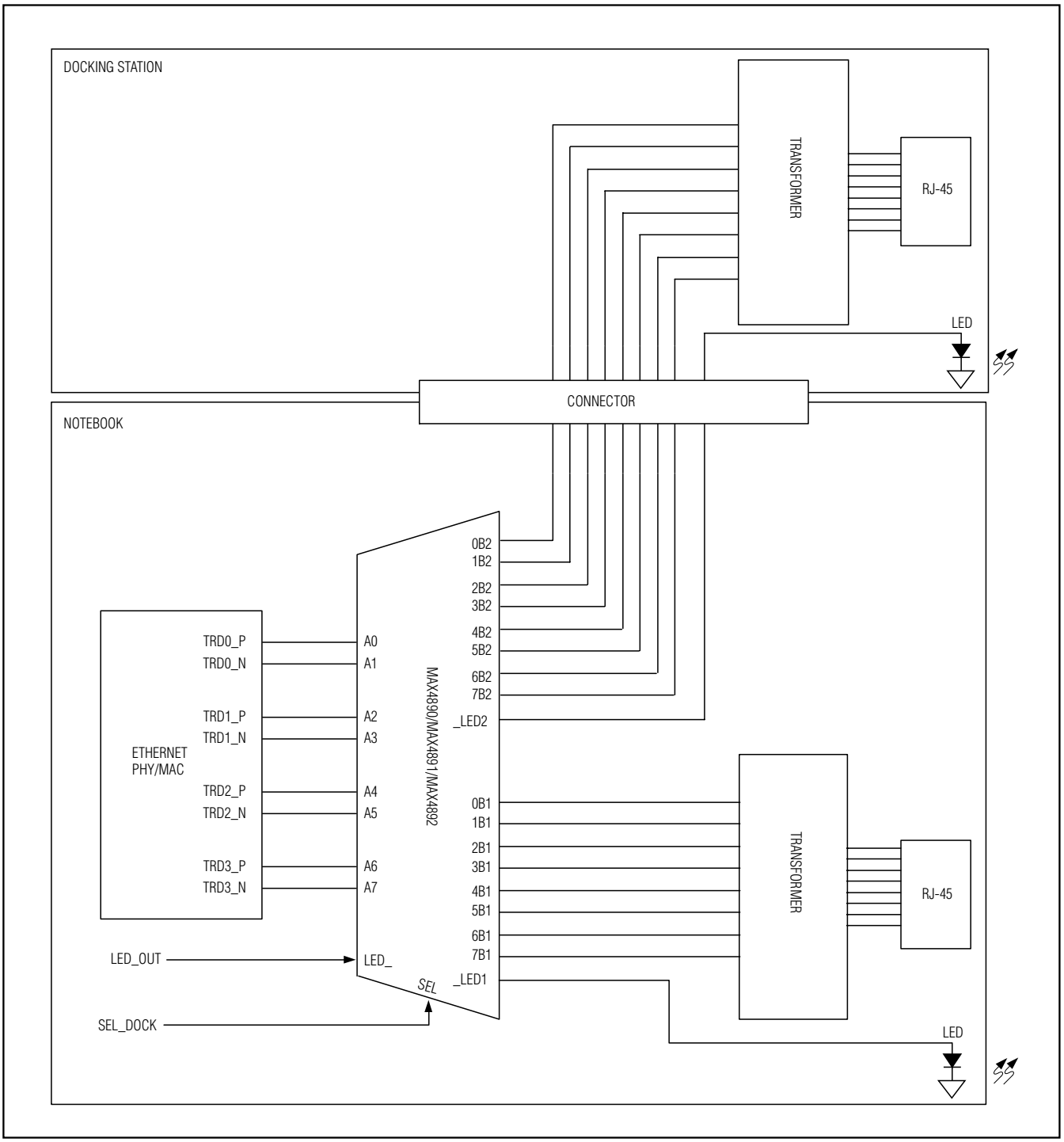
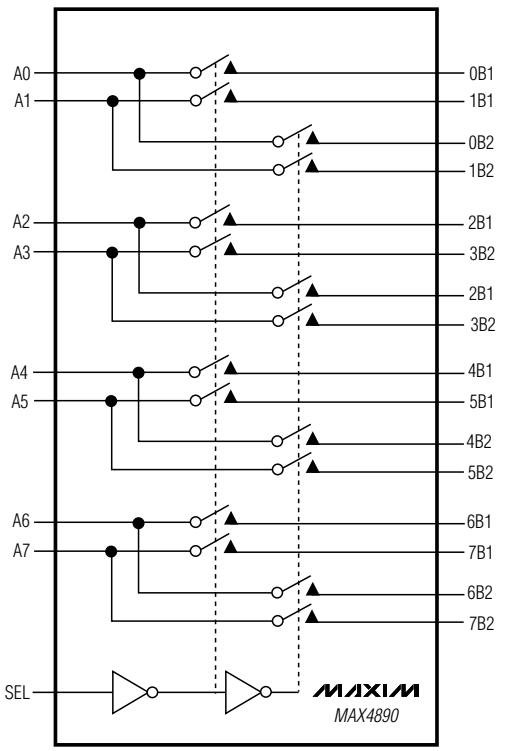


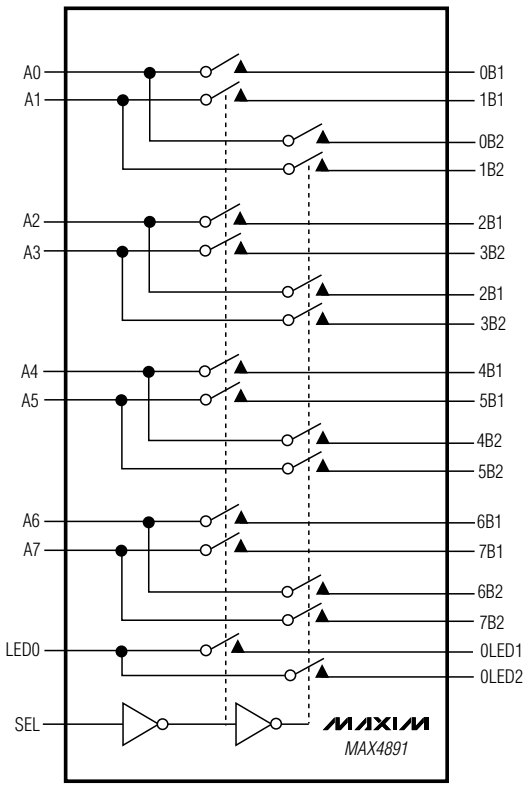
Figure 10. Typical Application for Line-Card Redundancy

Typical Operating Circuit

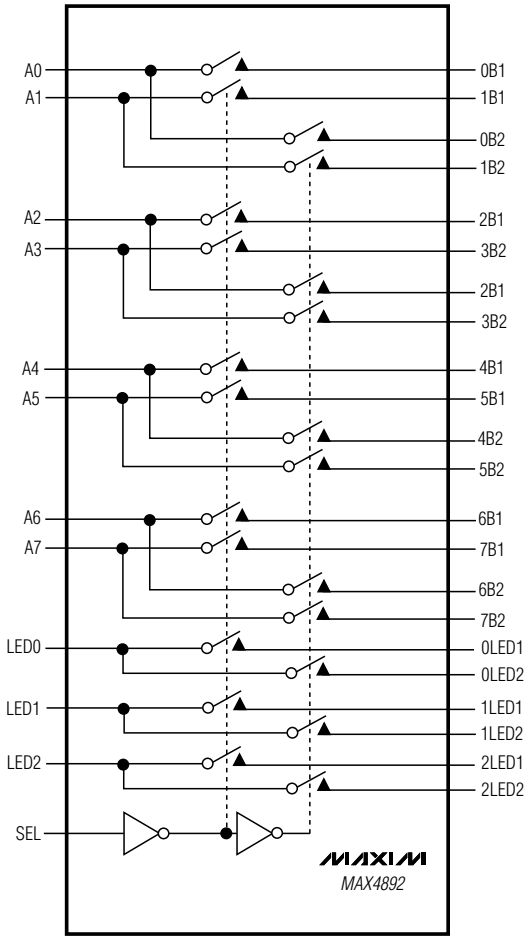


Functional Diagrams



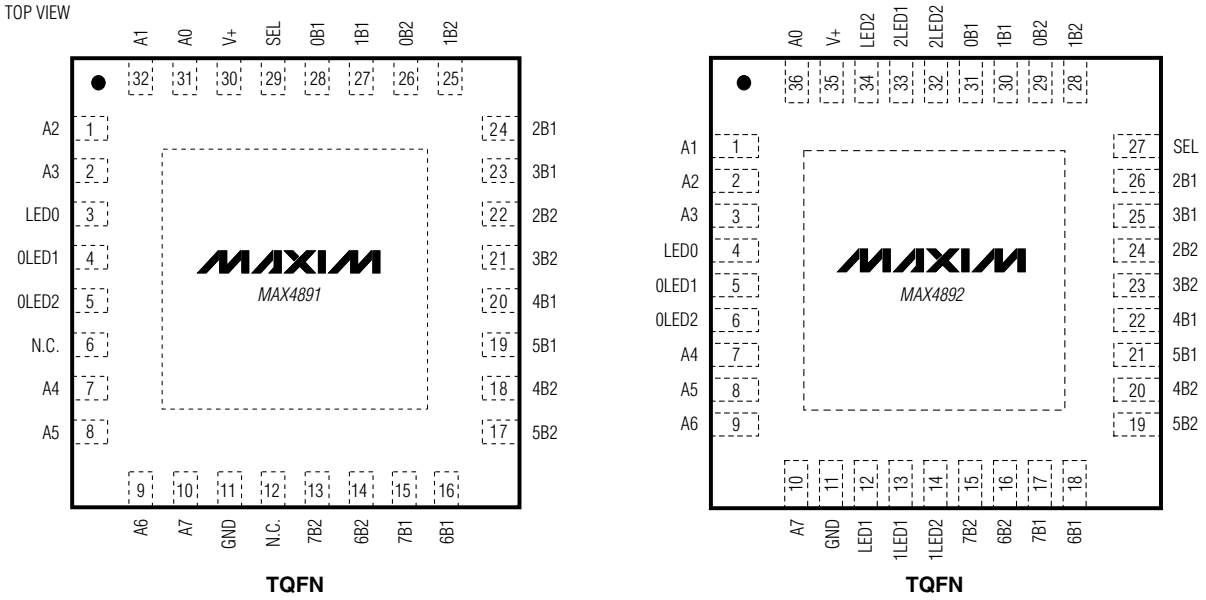


Functional Diagrams (continued)



10/100/1000 Base-T Ethernet LAN Switch

Pin Configurations (continued)



Chip Information

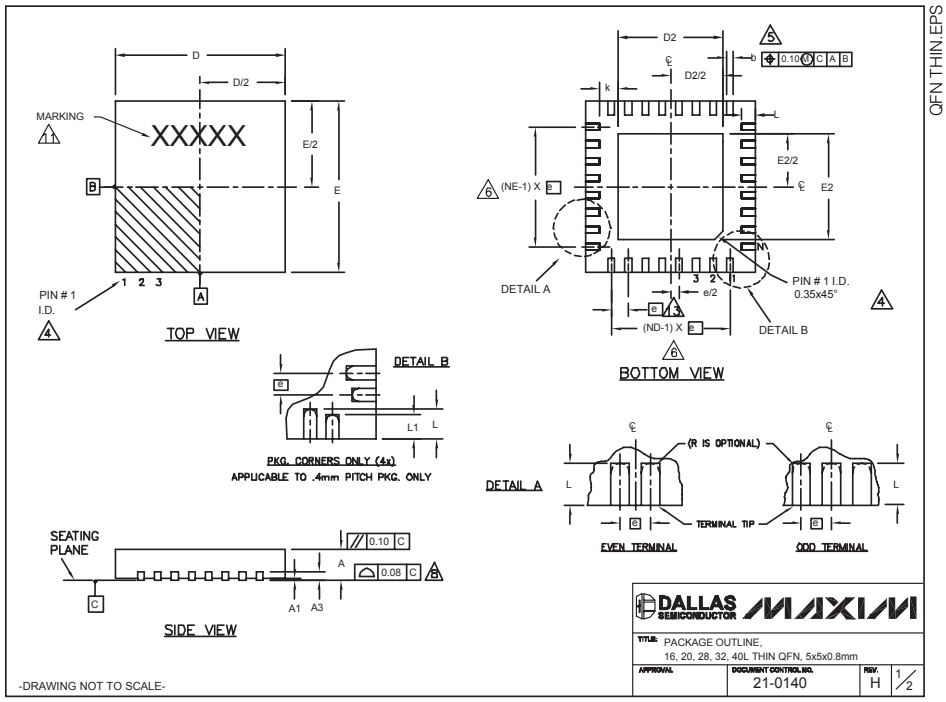
TRANSISTOR COUNT: 948

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL | DOCUMENT CONTROL NO. 21-0140 | REV. H | 1/2

-DRAWING NOT TO SCALE-

COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			L	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	±0.15	
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	**	YES

** SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3, AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

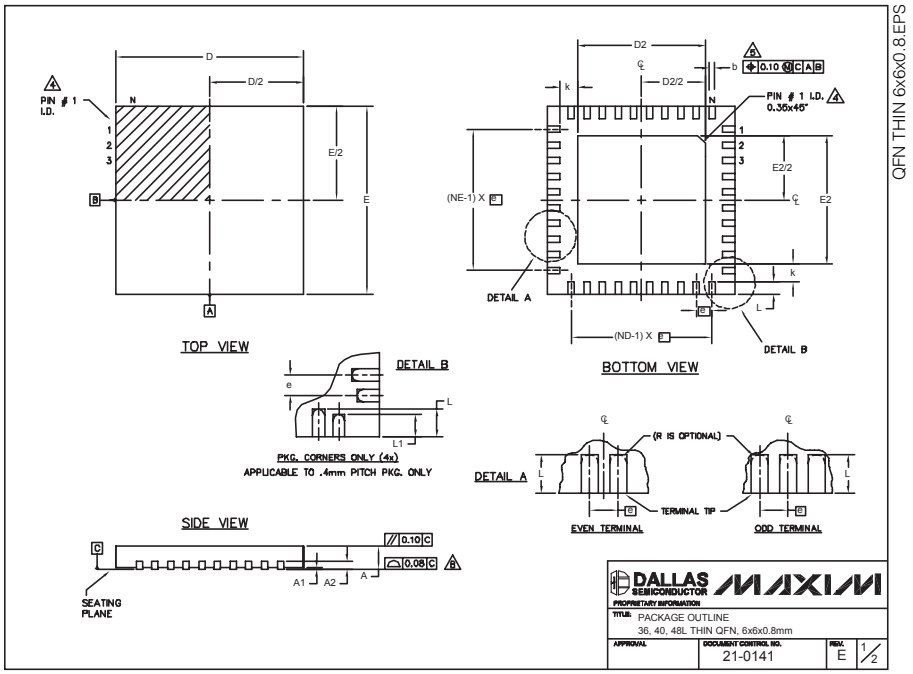
TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL | DOCUMENT CONTROL NO. 21-0140 | REV. H | 2/2

10/100/1000 Base-T Ethernet LAN Switch

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	0.35	0.45
L	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	–	–	–	–	–	–	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS							DOWN BONDS ALLOWED
PKG. CODES	D2			E2			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3666-1	3.60	3.70	3.80	3.60	3.70	3.80	NO
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80	YES
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80	NO
T4066-1	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4866-1	4.20	4.30	4.40	4.20	4.30	4.40	YES

NOTES:

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7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 36, 40, 48L THIN QFN, 6x6x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0141
REV. E
2/2